REMARKS/ARGUMENTS

Claims 1-12 and 21 are pending in this application. Claim 21 is newly added.

Claim Rejections – 35 U.S.C. § 103

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Ryoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). *See also In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970).

Further, "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations.*" (emphasis added) (MPEP § 2143). *If an independent claim is non-obvious under 35 U.S.C. §103, then any claim depending therefrom is non-obvious.* (emphasis added) *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In paragraph 3 of the Action, the Examiner has rejected Claims 1-9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,539,531 to Miller et al. (Miller) in view of U.S. Patent Application Publication No. 2002/0113619 to Wong et al. (Wong). In paragraph 4 of the Action, the Examiner has rejected claims 10-12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,829,031 to Lynch et al. (Lynch) in view of Wong.

Independent Claims 1 and 10 have been amended to remove the limitation that the characteristic on which the integrated circuit design optimization is based can be "latency." Claims 1 and 10 now recite only optimization based on "scalability" or "isochronous interconnect configuration."

The primary references, Miller and Lynch, fail to disclose, teach or suggest all the elements recited in Claims 1 and 10, specifically integrated circuit design optimization based on scalability or isochronous interconnect configuration. Applicants respectfully submit that the ancillary reference (Wong) does not cure the defects of Miller and Lynch.

Wong is cited for the disclosure of the use of integrated circuit design optimization based on "latency." However, Wong does not cure the defect of Miller or Lynch in reference to Claims 1 and 10 as it does not explicitly or implicitly teach or suggest integrated circuit design optimization based on scalability or isochronous interconnect configuration as recited in Claims 1 and 10. Claims 2-9, 11-12 and 21 are believed to be allowable based on their dependence upon allowable base claims.

Accordingly, the removal of all the pending rejections under 35 U.S.C. §103 is respectfully requested.

CONCLUSION

In light of the forgoing amendments and arguments, reconsideration of the claims is hereby requested, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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